

VIDEO AND SOUND IF AMPLIFIER FOR MONOCHROME TV RECEIVERS

The KA2913A, KA2917 are silicon monolithic integrated circuits designed for the VIF and SIF stage in B/W television receivers.

KA2913A: for Forward AGC type

KA2917: for Reverse AGC type

FUNCTION

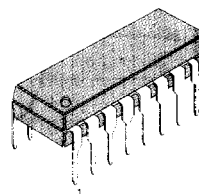
VIF stage

- Three controlled β amplifier stages
- Video demodulator controlled by the picture carrier
- Black noise and white noise inverter
- DC amplifier for RF AGC output
- Peak AGC

SIF stage

- Three controlled IF amplifier stages
- Quadrature detector

16 DIP



FEATURE

VIF stage

- High gain, wide band IF amplifier: 50dB (Typ.) at 45MHz
- Gain reduction with excellent stability: 55dB (Typ.) at 45MHz
- Excellent DG/DP characteristics: DG 7% (Typ.), DP 3.5 deg. (Typ.)
- Excellent S/N characteristics due to delayed 3-stage AGC action.
- Fast AGC action due to noise inverter and peak AGC.
- Switch off the video part with VTR switch.
- Dual differential AFT output

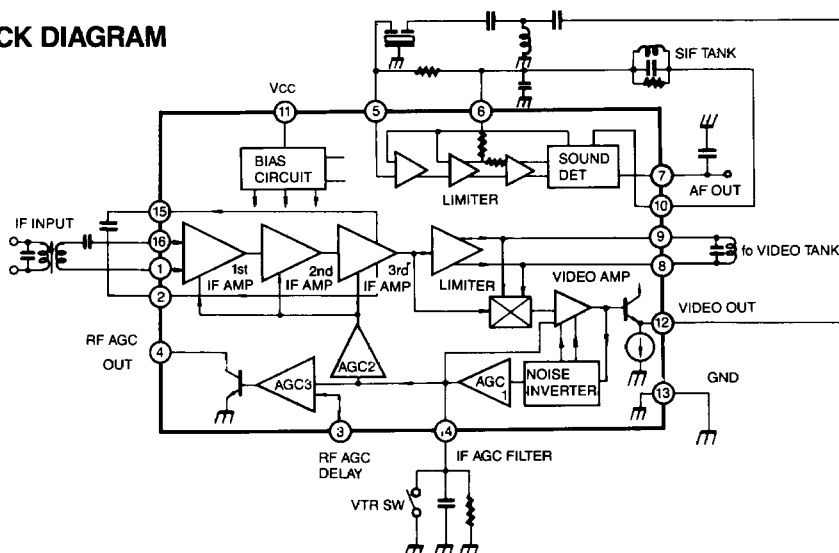
SIF stage

- Excellent limiter characteristics.
- Excellent AM rejection.
- Large undistorted audio output voltage with quadrature detector.

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2913A	16 DIP	- 20 ~ + 65°C
KA2917		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$)

Characteristic	Symbol	Value	Unit
Supply Voltage (Pin 11)	V_{CC}	15	V
Open Loop Voltage (Pin 4)	V_4	15	V
Video DC Output Current (Pin 12)	I_{12}	6	mA
Power Dissipation (Note)	P_D	1.4	W
Ambient Temperature	T_a	-20 ~ 65	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 ~ 150	$^\circ\text{C}$

Note: Derated above $T_a=25^\circ\text{C}$ in the proportion of 11.2 mW/ $^\circ\text{C}$.

ELECTRICAL CHARACTERISTICS

VIF Stage ($T_a=25^\circ\text{C}$, $V_{CC}=12\text{V}$, $V_{CC}=12\text{V}$, $f_p=45.75\text{MHz}$, $f_s=41.25\text{MHz}$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Recommended Supply Voltage	$V_{CC} (V_{11})$	—	10.8	12.0	13.2	V	—
Supply Current	$I_{CC} (I_{11})$	S_1 : On, S_3 : 2, S_5 : 2, S_4 : 1	35	50	65	mA	1
Video DC Output Voltage	V_{12}	S_1 : Off, S_3 : 2, S_5 : 2, S_4 : 1	5.2	5.5	5.8	V	1
Terminal Voltage 5	V_5	S_1 : On, S_3 : 2, S_5 : 2, S_4 : 1	3.5	4.4	5.3	V	1
Terminal Voltage 7	V_7	S_1 : On, S_3 : 2, S_5 : 2, S_4 : 1	4.6	6.0	7.2	V	1
RF AGC Residual Output Voltage	$V_4 \text{ Sat}$	S_1 : Off, S_3 : 2, S_5 : 2, S_4 : 1	—	—	0.5	V	1
RF AGC Leak Current	$I_4 \text{ Leak}$	S_1 : Off, S_3 : 1, S_5 : 1, S_4 : 2	—	—	1	μA	1
Video Sensitivity	$v_1 \text{ Pin-16}$	(Note 1)	60	150	250	μV_{rms}	2
AGC Range	$\Delta A \text{ (IF)}$	(Note 2)	60	64	—	dB	2
SYNC TIP Level Voltage	$V_{\text{SYNC}} (V_{12})$	(Note 3)	2.3	2.5	2.7	V	2
Maximum IF Input Voltage	$V_{\text{IN Max PIF}}$	(Note 4)	100	120	—	mV_{rms}	2
White Noise Threshold	$V_W \text{ TH} (V_{12})$	(Note 5)	5.8	6.2	6.6	V	2
White Noise Clamp Level	$V_{\text{WCL}} (V_{12})$	(Note 5)	3.7	4.1	4.5	V	2
Black Noise Threshold	$V_B \text{ TH} (V_{12})$	(Note 5)	1.4	1.6	1.8	V	2

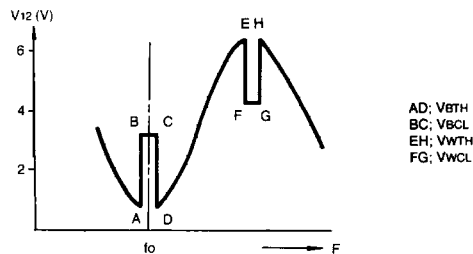
ELECTRICAL CHARACTERISTICS**VIF Stage ($T_a = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$, $f_p = 45.75\text{MHz}$, $f_s = 41.25\text{MHz}$)**

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit	Test Fig
Black Noise Clamp Level	V _B CL (V ₁₂)	(Note 5)		2.9	3.3	3.7	V	2
Video Frequency Response	f _{ew}	(Note 6)		4.5	5.5	—	MHz	3
Suppression of Carrier	CL	(Note 7)		40	50	—	dB	4
Suppression of 2nd Carrier	I _{2nd}	(Note 8)		40	50	—	dB	4
Suppression of Sound Carrier/ Color Subcarrier	I ₉₂₀	(Note 9)		33	38	—	dB	4
Differential Phase	DP	(Note 10)		—	3.5	5	deg	5
Differential Gain	DG	(Note 10)		—	7	10	%	5
VIF Input Impedance	R _{IN} (VIF)	(Note 11)		1.5	3.0	6.0	KΩ	6
	C _{IN} (VIF)			—	3.0	10.0	pF	
Max. Available Current	I ₄ MAX	(Note 12)	KA2917	0.3	—	—	mA	1
			KA2913A	7	—	—	mA	
RF AGC Delay Point Range	V _{IN} Delay	(Note 13)		5.0	7.0	9.0	V	2
Video Output Level	V _{OUT}	(Note 14)		2.25	2.5	2.75	V	2

ELECTRICAL CHARACTERISTICS**SIF Stage ($T_a = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$, $f_p = 45.75\text{MHz}$, $f_s = 41.25\text{MHz}$)**

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
SIF Output Voltage	S_{OUT}	(Note 15)	200	400	600	mV _{rms}	3
Input Limiting Voltage	$V_{IN} \text{ (Lim)}$	(Note 16)	—	200	400	μV_{rms}	8
AM Rejection Ratio	AMR	(Note 17) $R_L = \infty$ $R_D = \infty$	40	45	—	dB	8
Recovered Output Voltage	V_{OD}	(Note 18) $R_L = \infty$ $R_D = \infty$	0.5	0.75	—	V _{rms}	8
Total Harmonic Distortion	THD	(Note 18) $R_L = \infty$ $R_D = \infty$	—	1.0	2.0	%	8
Max. Audio Output Voltage	V_{OM}	(Note 19)	4.0	—	—	V _{p.p}	8
SIF Input Impedance	$R_{IN} \text{ (SIF)}$		10	20	30	K Ω	7
	$C_{IN} \text{ (SIF)}$		—	3	10	pF	
Audio Output Impedance	$R_{O(AFI)}$	(Note 20)	10	15	20	K Ω	9

- Note 1) V_{AGC} (TP14 EXT. Applying voltage)=11.5V
 VIF in: $f=45.75\text{MHz}$, 1kHz 30% AM modulation
 Adjust VIF input level U_i so that the detected output of TP12C with high impedance probe will be $0.8V_{p-p}$ and measure the input level.
- Note 2) $V_{AGC}=4V$
 Measure VIF input level U_i same as note 1
- $$\Delta A = 20 \log \frac{U_i'}{U_i} (\text{dB})$$
- Note 3) VIF in: $f=45.75\text{MHz}$ CW 15mVrms
 Measure the DC level of TP12A.
- Note 4) VIF in: $f=45.75\text{MHz}$ APL100%, 87.5% AM modulation.
 TP14: open
 (1) Adjust VIF input level 50mV_{p-p} and measure the detected output level U_{o-p-p}
 (2) Then increase the input level so that the detected output level will be $1.1 \times U_{o-p-p}$ and measure the input level.
- Note 5) $V_{AGC}=8V$
 VIF in: $f=45.75\text{MHz} \pm 10\text{MHz}$ variable or sweep 15mVrms measure DC level of TP12A



- Note 6) $V_{AGC}=8V$
 SG₁: 45.75MHz CW
 SG₂: 45.65-27MHz variable
 (1) Setting output of SG₁ so that the DC level of TP12A will
 (2) Setting output of SG₂ (45.65MHz) so that the AC level of TP12A will be $0.5V_{p-p}$
 (3) Decreasing frequency of SG₂ until the AC level of TP12A will be $0.35V_{p-p}$ (-3dB of $0.5V_{p-p}$) then read
 $f_{SG2} = F f_{BW} = 45.75 - F \text{ MHz}$
- Note 7) SG₁: 45.75MHz, 1kHz 80% AM modulation 100mVrms
 SG₂, SG₃: off
 Setting V_{AGC} so that the output AC level of TP12A will be $2.7V_{p-p}$
 Measure CL of TP12A after setting to 0% AM of SG₁
- Note 8) Measure 2nd of TP12A same as Note 9
- Note 9) $V_{AGC}=8V$
 SG₁: 45.75MHz (P: picture) 100mVrms
 SG₂: 41.25MHz (S: sound) 32mVrms (-10dB of SG₁)
 SG₃: 42.17MHz (C: chroma) 32mVrms (-10dB of SG₁)
 (1) Setting V_{AGC} so that the output tip level (lower) of TP12A will be 3.0V DC
 (2) Measure the level difference (dB) between the C-level and 920KHz level
- Note 10) $V_{AGC}=8V$
 VIF in: $f=45.75\text{MHz}$ video signal (RAMP) 87.5% AM 100mV_{p-p}
 Setting ATT so that the SYNC TIP level of TP12A will be 2.5V DC measure DP and DG.

Note 11) $V_{AGC} = 5V$ $f = 45.75MHz$
Measure R_{IN} , C_{IN}

Note 12) S_1 : On, S_3 : 2, S_5 : 1 S_4 : 1 for 2917
2 for 2913A

Note 13) TP14: Open
VIF in: 45.75MHz CW 20mVrms
(1) Adjust the voltage of Terminal 3 so that the voltage of Terminal 4 will be 6.0V DC
(2) Measure the Terminal voltage 3

Note 14) TP14: Open
VIP in: 45.75MHz 100% APL 87.5% AM modulation signal amplitude 50mV_{p-p}, measure the detected output voltage (white peak to SYNC TIP)

Note 15) TP14: Open
SG₁: 45.75MHz CW 100mVrms
SG₂: 41.25MHz CW 25mVrms
Measure SIF (4.5MHz) output voltage at TP12A

Note 16) SIF IN: $f = 4.5MHz$ FM $f_{MOD} = 400Hz$ $\Delta f = \pm 25kHz$
(1) Adjust SIF input level 100mV_{p-p} and measure the detected output level V_{OS}
(2) Then decrease the input level so that the detected output level will be 3dB down of V_{OS} and measure the input level.

Note 17) SIF IN: $f = 4.5MHz$ FM $f_{MOD} = 400Hz$ $\Delta f = \pm 25kHz$
AM 30%
Input level $V_{INS} = 100dB\mu$

Note 18) SIF IN: $f = 4.5MHz$ FM $f_{MOD} = 400Hz$ $\Delta f = \pm 25kHz$
Input level $V_{INS} = 80dB\mu$

Note 19) SIF in: $f = 4.4-4.6MHz$ variable or sweep measure the output DC voltage change

Note 20) SIF IN: $f = 4.5MHz$ FM $f_{MOD} = 400Hz$ $\Delta f = \pm 25kHz$
Input level $V_{INS} = 80dB\mu$
(1) Measure the detected output voltage V_{OA} with $R_X = \infty$
(1) Then, adjust R_X so that the detected output voltage will be $\frac{V_{OA}}{2}$ and measure R_X .

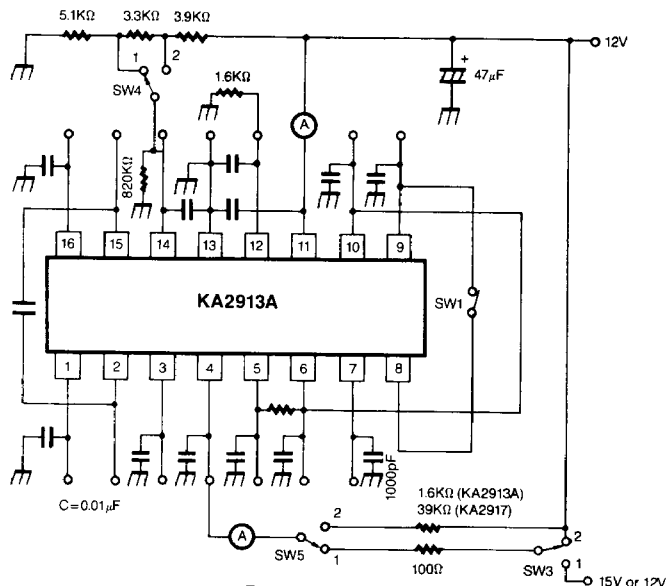


Fig. 1

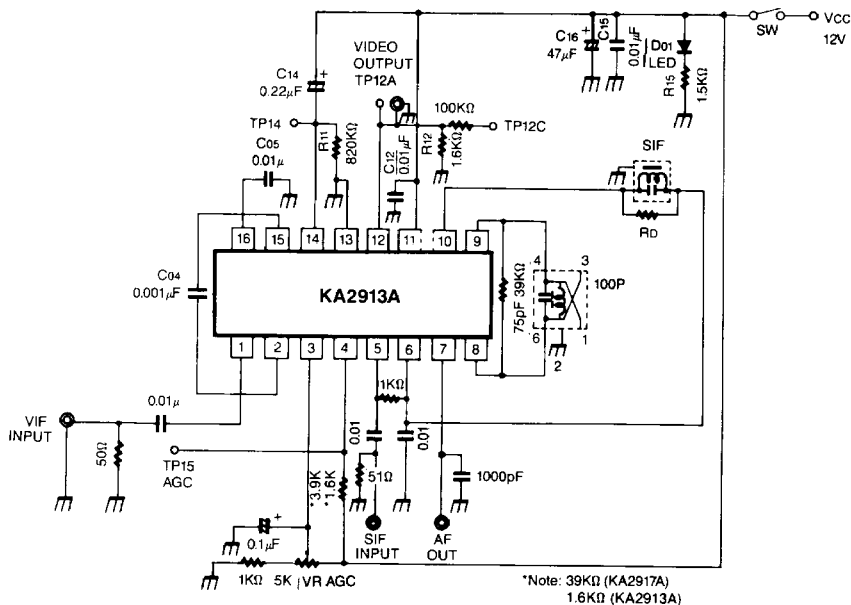


Fig. 2

3. VIDEO FREQUENCY RESPONSE & SIF OUTPUT VOLTAGE TEST CIRCUIT

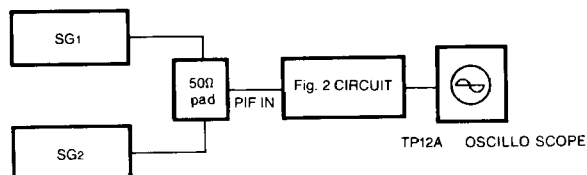


Fig. 3

4. INTER MODULATION TEST CIRCUIT

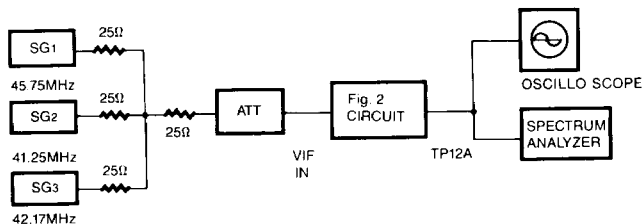
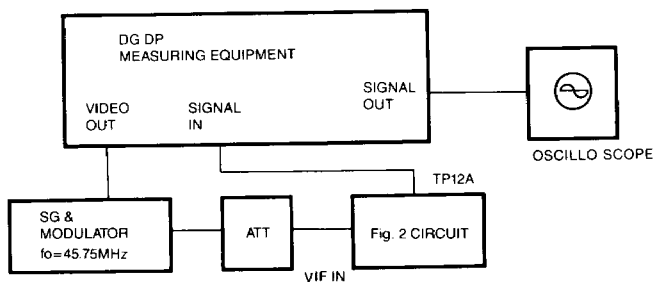


Fig. 4

5. DG, DP TEST CIRCUIT



APL: 50%
ATT: ADJUST SYNC TIP LEVEL TO DC2.5V

Fig. 5

6. INPUT IMPEDANCE TEST CIRCUIT

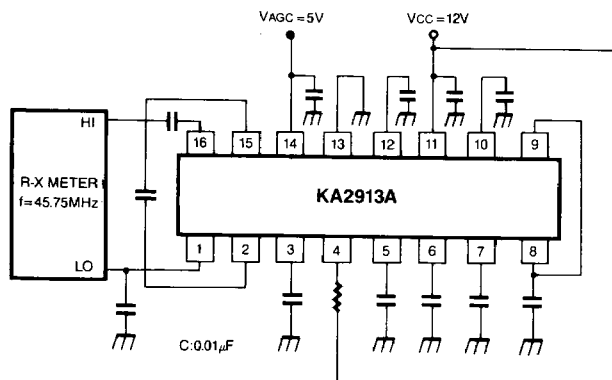


Fig. 6

7. SIF INPUT IMPEDANCE TEST CIRCUIT

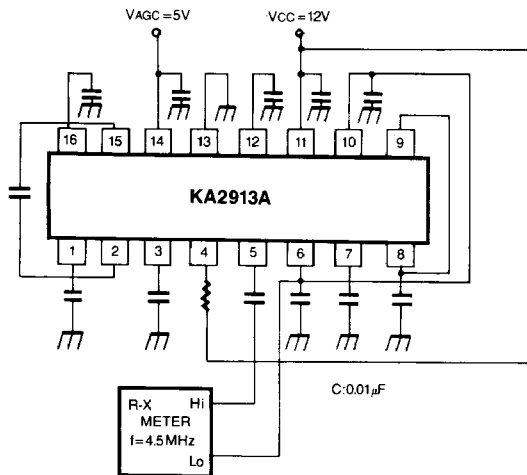


Fig. 7

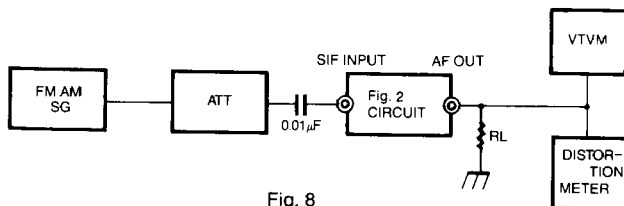
8. V_{IN} (LIM), AMR, V_{OD} , THD, V_{OM} TEST CIRCUIT

Fig. 8

TYPICAL APPLICATION CIRCUIT

